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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,253	03/29/2004	Hau-Tai Shieh	TSMC2003-1245(N1280-00220	2744

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IP DEPARTMENT  
ONE LIBERTY PLACE  
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EXAMINER .
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NGUYEN, DANG T

ART UNIT	PAPER NUMBER
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2824

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No. 10/812,253	Applicant(s) SHIEH, HAU-TAI	
	Examiner Dang T. Nguyen	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 March 2005.  
 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-21 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☒ The drawing(s) filed on 29 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \*    c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 03/29/05.  
Claims 1, 8 and 16 have been amended. Claims 1, 8 and 16 are independent claims.  
Claims 1-21 are pending on this application.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**Claims 1 - 21 rejected under 35 U.S.C. 102(b) as being anticipated by  
Leung, Pub.No.: US 2001/0007538A1.**

**Regarding independent claim 1**, Fig. 1 of Leung discloses a method for refreshing a memory system having a predetermined number of memory blocks [1000 – 1127], comprising: providing a system refresh signal for refreshing the memory system, the system refresh signal being used as a first refresh request signal for refreshing a first memory block (page 4 paragraph [0047] lines 7 – 10); sequentially refreshing one or more subsequent memory blocks of the memory system (page 4 paragraph [0047]) such that no two memory blocks are refreshed at the same time (On page 5 paragraph 0060, discloses request refresh in daisy-chained manner, Leung clearly teaches the memory block is refresh according the daisy-chained manner and that mean each block of the memory blocks is refreshed one at a time according to the refresh signal.

Furthermore, nowhere in the disclosures of Leung discloses the memory blocks will be refreshed at the same time), wherein all the memory blocks are refreshed within a retention cycle of the memory system (page 1 paragraph [0004]).

**Regarding dependent claim 2**, Figure 1 of Leung discloses wherein the providing further includes generating the system refresh signal by a refresh timer [102] coupled to the first memory block [DRAM BLOCK 1000].

**Regarding dependent claim 3**, Figure 1 of Leung discloses wherein the sequentially refreshing further includes sequentially generating one or more refresh request signals for the subsequent memory blocks (Page 4, paragraph [0047] lines 20-23).

**Regarding dependent claim 4**, Figure 2 of Leung discloses wherein the sequentially refreshing further includes providing a refresh request signal by a refresh control circuit in each subsequent memory block to its immediately subsequent memory block while it is undergoing a refresh operation (Pages 4 and 5, paragraphs [0053 – 0055]).

**Regarding dependent claim 5**, Leung discloses wherein the sequentially refreshing further includes generating a refresh command based on the refresh request signal for refreshing each memory block (page 2 paragraph [0013]).

**Regarding dependent claim 6**, Leung discloses wherein the refresh commands for the memory blocks do not overlap in timing (paragraph [0004] for disclosing the cycle time for each refresh operation of a DRAM cell to prevent the refresh access from

interfering with the external access and the overlap in timing) and (Page 2, paragraph [0013]).

**Regarding dependent claim 7**, Leung discloses wherein the refresh requests do not overlap in timing (Pages 1 and 2, paragraphs [0004 and 0013]).

**Regarding independent claim 8**, Fig. 1 of Leung discloses a memory system comprising: a first memory block coupled to a refresh timer ([102] connects to [DRAM BLOCK 1000]); and one or more subsequent memory blocks without refresh timer contained therein (See Fig. 1, only [BLOCK 1000] coupled to a refresh timer) wherein the refresh timer generates a system refresh signal for refreshing the memory system (Page 2 paragraph [0013]), and wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks (page 2 paragraph [0014] and [0011]), such that no two memory blocks are refreshed at the same time (On page 5 paragraph 0060, discloses request refresh in daisy-chained manner, Leung clearly teaches the memory block is refresh according the daisy-chained manner and that mean each block of the memory blocks is refreshed one at a time according to the refresh signal. Furthermore, nowhere in the disclosures of Leung discloses the memory blocks will be refreshed at the same time).

**Regarding dependent claim 9**, Fig. 1 of Leung discloses wherein the refresh controller of the first memory block receives the system refresh signal generated by the refresh timer ([102] and page 4, paragraph [0047]).

**Regarding dependent claim 10**, Leung discloses wherein the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block (Page 2, paragraph [0011]).

**Regarding dependent claim 11**, Fig. 1 of Leung discloses wherein the refresh controller of each memory block generates a refresh request [RFREQ] for an immediately subsequent memory block when the memory block it belongs to is being refreshed (Page 4, paragraph [0047]).

**Regarding dependent claim 12**, Leung discloses wherein the refresh requests generated do not overlap in timing (Pages 1 and 2, paragraphs [0004 and 0013]).

**Regarding dependent claim 13**, Leung discloses wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to (Page 2, paragraph [0013]).

**Regarding dependent claim 14**, Leung discloses wherein the refresh commands generated do not overlap in timing (Pages 1 and 2, paragraphs [0004 and 0013]).

**Regarding dependent claim 15**, Fig. 1 of Leung discloses wherein the refresh controller provides a refresh address [101].

**Regarding independent claim 16**, Fig. 1 of Leung discloses a dynamic random access memory system comprising: a first memory block [1000] coupled to a refresh timer [1002]; and one or more subsequent memory blocks without refresh timers contained therein (See Fig. 1, only [BLOCK 1000] coupled to a refresh timer), wherein the refresh timer generates a system refresh signal for refreshing the memory system

(page 2 paragraph [0013]), and wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks (page 2, paragraphs [0014 and [0011]), such that no two memory blocks are refreshed at the same time (page 2 paragraph [0014] and [0011]), such that no two memory blocks are refreshed at the same time time (On page 5 paragraph 0060, discloses request refresh in daisy-chained manner, Leung clearly teaches the memory block is refresh according the daisy-chained manner and that mean each block of the memory blocks is refreshed one at a time according to the refresh signal. Furthermore, nowhere in the disclosures of Leung discloses the memory blocks will be refreshed at the same time).

**Regarding dependent claim 17**, Fig. 1 of Leung discloses wherein the refresh controller of the first memory block receives the system refresh signal generated by the refresh timer ([102] and page 4, paragraph [0047]).

**Regarding dependent claim 18**, Fig. 1 of Leung discloses wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to and a refresh request [RFREQ] for an immediately subsequent memory block when the memory block it belongs to is being refreshed (page 4, paragraph [0047]).

**Regarding dependent claim 19**, Fig. 1 of Leung discloses wherein the refresh requests generated do not overlap in timing (Pages 1 and 2, paragraphs [0004 and 0013]).

**Regarding dependent claim 20**, Fig. 1 of Leung discloses wherein the refresh commands generated do not overlap in timing (Pages 1 and 2, paragraphs [0004 and 0013]).

**Regarding dependent claim 21**, Fig. 1 of Leung discloses wherein the refresh controller provides a refresh address [101].

### ***Response to Arguments***

3. Applicant's arguments filed 3/29/05, have been fully considered but they are not persuasive.

Under remarks on page 8 and 9, applicant argued that the refresh of memory blocks in daisy-chain manner taught by Leung does not guarantee that two memory banks cannot be refreshed at the same time, and is possible for the two or more memory blocks to be refreshed at the same time if refresh of bank "a" is delayed one clock cycle and refresh of bank "b" which is daisy-chained to bank "a" is not delay, both memory banks will be refreshed simultaneously. However, "if", "does not guarantee" and "possible" from the argument above are assumption or opinion only, and not the fact. Therefore, the argument is not persuasive.

On page 5 paragraph 0060, discloses request refresh in daisy-chained manner, Leung clearly teaches the memory block is refresh according the daisy-chained manner and that mean each block of the memory blocks is refreshed one at a time according to the refresh signal. Furthermore, nowhere in the disclosures of Leung discloses the

memory blocks will be refreshed at the same time if a delay occurs. Accordingly, Leung from previous office action is applying to this office action.

### ***Conclusion***

**4. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

### ***Contact Information***


**5.** Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or [EBC@uspto.gov](mailto:EBC@uspto.gov).

Dang Nguyen 5/23/2005

  
**ANH PHUNG**  
**PRIMARY EXAMINER**